

**VERY FAST LOAD TRANSIENT RESPONSE  
WITH THE NEW LPR30 APPLICATION**

**INTRODUCTION**

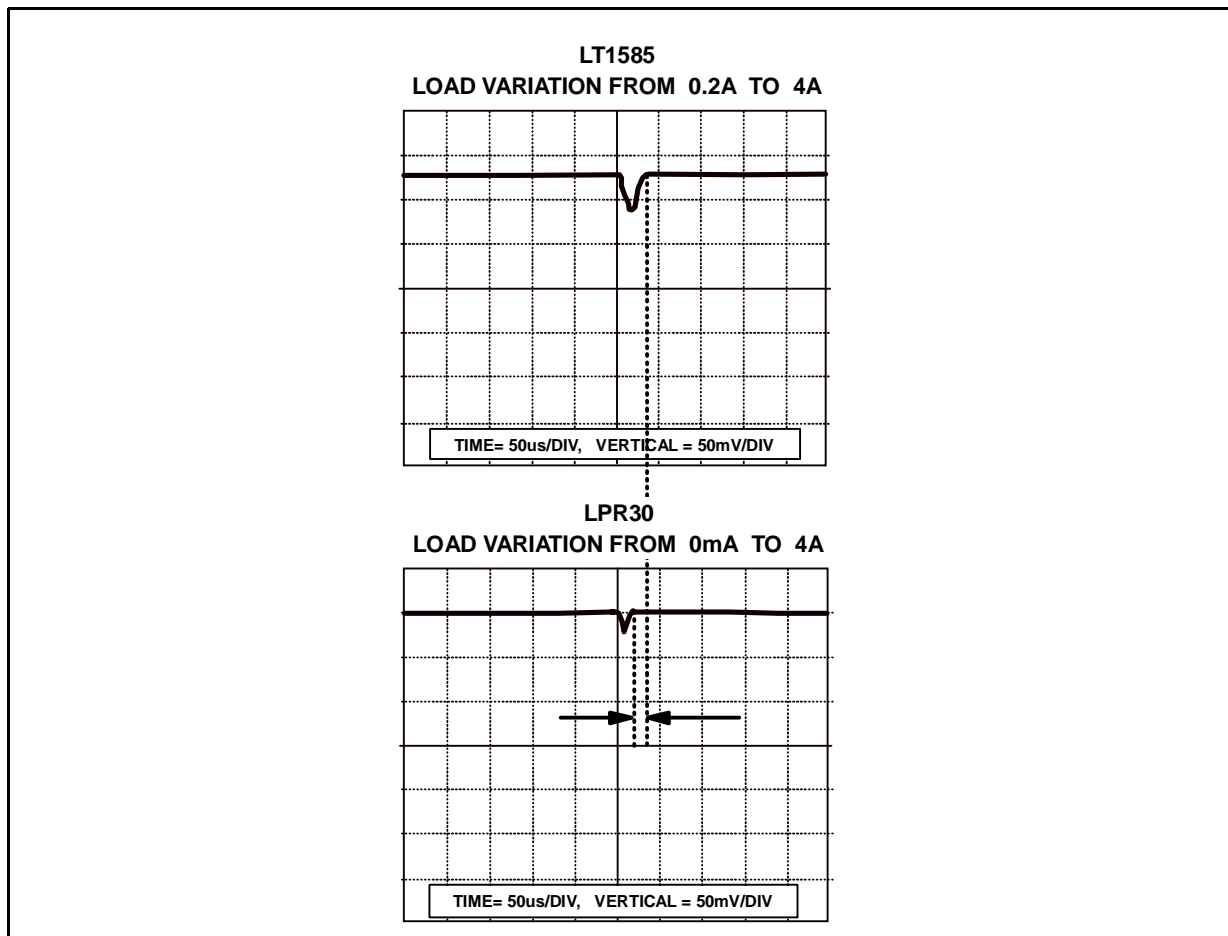
Some applications requires high performances power supply characteristics in terms of fast recover to properly work. In particular it happen in the sequential system, where if an unexpected and high current absorption happens the output voltage go down due to the slow power supply response. If in the system there are microprocessor or counters, functionality problems could happen. Some companies suggest integrated solutions, but the performances are not optimum due to recovery times around 40µs, with output current medium or low and high dropout voltage ( as it is shown in figure 1, LT1585 performances ).

Using the LPR30 it is easy to realize power supply system with improved performances thanks to the high flexibility given by this device . In fact using an external Power Mosfet , the ctm can use components with very low R<sub>LOAD</sub>.

In this way it is possible to supply current more than 10A, with lower dropout voltage.

Another important feature of the LPR30 is the un compensated internal ERROR AMPLIFIER; which allows for realization of an optimized external compensated network in terms of faster response.

**Figure 1. LT1585 and LPR30 Load Variations (R<sub>2</sub> = 50Ω, Cout = 220µF).**



# AN964 APPLICATION NOTE

## CIRCUIT DESCRIPTION

The electric schematic is shown in Figure 2.

Figure 2. Electric Schematic.

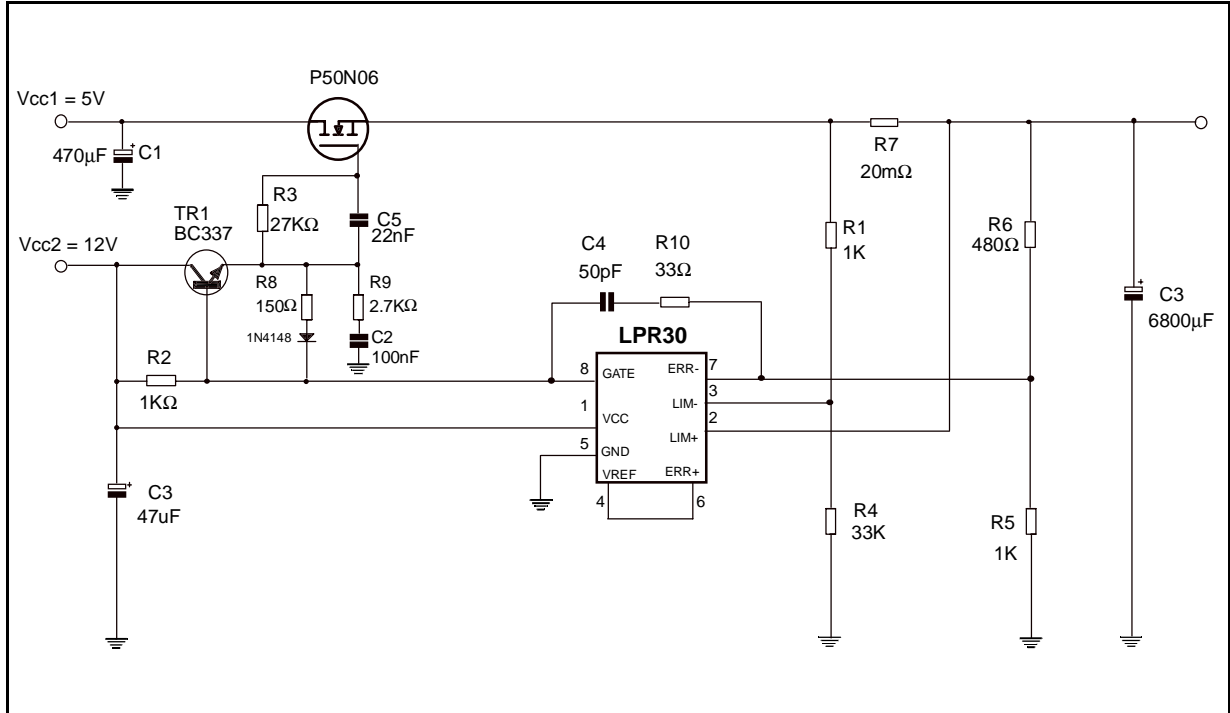


Table 1. Components description

Resistor	Value	Capacitor	Value
R1	1kΩ	C1	470µF
R2	1kΩ	C2	100nF
R3	27Ω	C3	6800mF
R4	33kΩ	C4	50pF
R5	1kΩ	C5	22nF
R6	480Ω	C6	47mF
R7	20mΩ		
R8	150Ω		
R9	2.7kΩ		
R10	33Ω		

In the circuit there are two different compensation ;

- the first one implements the current limit amplifier,
- the second one implements the error amplifier. The first compensation is given by R3, R8, R9, C2, D1 and TR1 .

The transistor TR1 is utilized to decrease the R2 resistor value; consequently it follows that there is a reduction of the total response time.

The second compensation is given by R10, C4 and C3.

In particular C3 in combination with  $R_{LOAD}$  constitutes the domination pole. It is important that the "constant time" associated with  $C3 \cdot R_{LOAD}$  is  $\tau \geq 1.8ms$ . So if the ctm needs a  $V_{out} \geq 3.3V$  and  $I_{OUTMAX} =$

15A it follows :

$$R_{LOADMIN} = \frac{V_{out}}{I_{OUTmax}}$$

then

$$\frac{3.3}{15} = 0.22\Omega$$

and

$$\frac{C3 > (1.8 \cdot 10^{-3})}{R_{LOADmin}} 8.200mF$$

R10 and C4 decrease the amplifier error Gain at the high frequencies, while C5 improves the fast response.

Here below in figure n. 3 is shown the typical application demoboard.

**HINTS...**

In order to allow the complete Power MOSFET driving , V2 must be greater than  $V_{OUT} + V_{GSat} \cdot R1$  and R4 value are calculated in according to  $I_{OUTMAX}$  and  $I_{OUTC.C}$  performances. Looking to the power dissipated at point A is:

$$P_{DA} = (V_{in} - V_{out} - R_{sense} \cdot I_{max}) \cdot I_{max}.$$

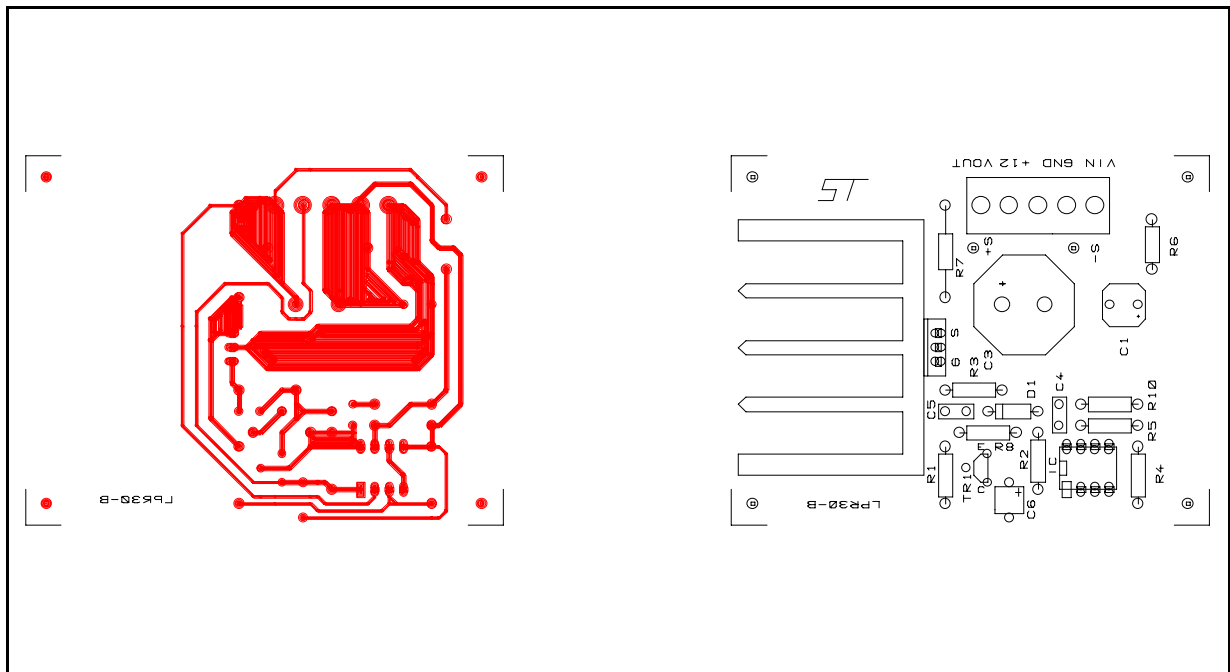
While the power dissipated at point B is

$$P_{DB} = (V_{in} - R_{sense} \cdot I_{sc}) \cdot I_{sc} \cong V_{in} \cdot I_{sc}.$$

In the operating mode it is good choice to impose  $P_{DB} \leq P_{DA}$  to avoid a larger heatsink dimensioning in short circuit condition. If we let  $P_{DA} = P_{DB}$  , we obtain:

$$I_{sc} = \frac{(V_{in} - V_{out} - R_{sense} \cdot I_{max}) \cdot I_{max}}{V_{in}}$$

**Figure 3 . Typical Application Demoboard.**



## AN964 APPLICATION NOTE

Figure 4 reports the foldback limitation characteristic. In some applications it is not possible to impose  $P_{DB} \leq P_{DA}$  because a high ratio  $I_{max}/I_{sc}$  implies an higher drop on the  $R_{sense}$ .

In fact :

$$R_{sense} \cdot I_{sc} = 50 \cdot 10^{-3} \cdot \frac{R1 + R4}{R4} > 50mV$$

$$\frac{R_{sense} > 50mV}{I_{sc}}$$

and then

$$R_{sense} \cdot I_{max} = V_{sense} > 50mV \cdot \left( \frac{I_{max}}{I_{sc}} \right)$$

So the starting point to determinate all the components to be used is to impose the dissipation in short circuit condition :

$$P_{D-B} = (V_{in} - R_{sense} \cdot I_{sc}) \cdot I_{sc} \cong V_{in} \cdot I_{sc} > V_{in} \cdot 50mV \cdot I_{max} / V_{sense}$$

and then

$$1) \quad V_{sense} > 50mV \cdot \left[ \frac{(V_{in} \cdot I_{max})}{P_{D-B}} \right]$$

$$2) \quad R_{sense} = \frac{V_{sense}}{I_{max}}$$

$$3) \quad R_{ONmax} \leq \left[ \frac{(V_{drop} - V_{sense})}{I_{max}} \right] \text{ and so the PowerMOSFET.}$$

4) Now we can calculate the R1 and R4 resistors.  $(R1 + R4) = \frac{V_{out} + V_{sense}}{V_{out} + 50mV} - 1$  and so imposing the R1 we can determinate the R4

$$5) \quad I_{sc} = \left( \frac{50mV}{R_{sense}} \right) \cdot \left[ \frac{(R1 + R4)}{R4} \right]$$

## PERFORMANCES

Figure 5 shows the Load Transient Response of the power supply when the load increases from 0A to 10A .

It is possible to see response times extremely short (around 1 $\mu$ s), even if we start from no-load condition. Consequently the Output Voltage variations are extremely reduced. It is possible to reduce this Load Variation even further by increasing the Output Capacitor (C3) value.

Figure 4.

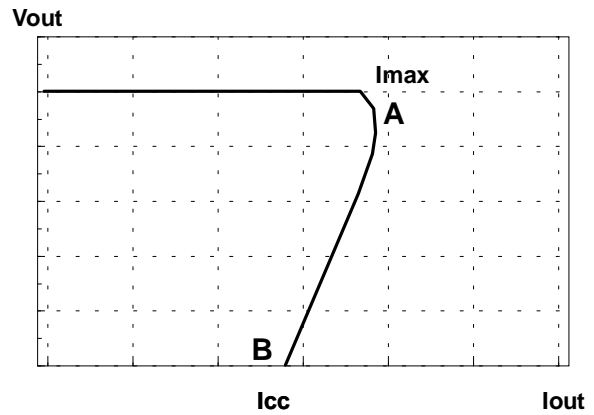
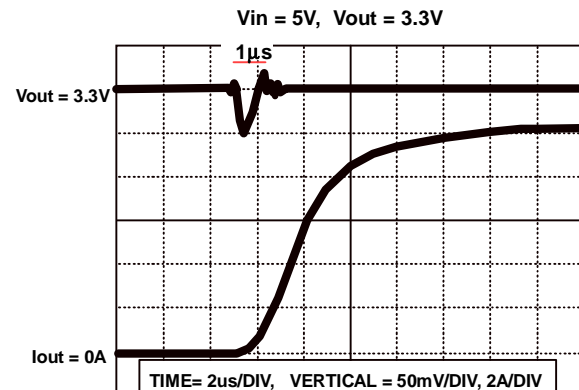


Figure 5.

## LOAD VARIATION FROM 0A TO 10A



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